

IN THE CLAIMS

This listing of Claims shall replace all prior versions, and listings, of claims in the application:

1. (Currently amended) An ~~request tracking data prefetch~~ apparatus for a computer system, comprising:
 - a prefetcher coupled to a ~~first high latency~~ memory for a processor of the computer system, the memory having a first latency;
 - a tracker within the prefetcher and configured to recognize processor accesses to a plurality of cache lines within a ~~low latency second~~ memory having a second latency less than the first latency, the second memory operable to supply data to the processor responsive to processor data requests, wherein the processor accesses form a stream-type sequential access pattern, and wherein further the tracker is configured to use a bit vector to predictively load a target cache line indicated by the stream-type sequential access pattern from the ~~high latency~~ first memory into the ~~low latency~~ second memory for the processor in preparation for the target cache line being requested by the processor as part of the stream-type processor access pattern.
2. (Currently amended) The apparatus of claim 1, wherein the tracker includes a tag configured to recognize accesses to corresponding cache lines of the ~~high latency~~ first memory by the processor.
3. (Currently amended) The apparatus of claim 2, wherein a plurality of accesses by the processor to the ~~high latency~~ first memory as recognized by the tag are used by the

tracker to determine the target cache line for a predictive load into the ~~low latency~~second memory.

4. (Currently amended) The apparatus of claim 3, wherein consecutive accesses by the processor to adjacent cache lines of the ~~high latency~~first memory are used to determine the target cache line for a predictive load into the ~~low latency~~second memory, and wherein the adjacent cache lines have adjacent addresses.

5. (Currently amended) The apparatus of claim 1, wherein the ~~high latency~~first memory comprises a memory block of a plurality of memory blocks of the computer system.

6. (Currently amended) The apparatus of claim 5, wherein the ~~high latency~~first memory comprises a four kilobyte page of system memory of the computer system.

7. (Currently amended) The apparatus of claim 5, wherein the tracker includes a tag configured to monitor a sub portion of the ~~high latency~~first memory for accesses by the processor.

8. (Currently amended) The apparatus of claim 1, wherein the ~~high latency~~first memory is a system memory of the computer system.

9. (Currently amended) An ~~request tracking data prefetch~~ apparatus for a computer system, comprising:

a processor;

a system-first memory coupled to the processor, wherein the first memory having a first latency;

a prefetch unit coupled to the system-first memory;

a plurality of trackers included in the prefetch unit, wherein the trackers are respectively configured to recognize processor accesses to pages of the system-first memory, and configured to recognize accesses to cache lines within a cache-second memory having a second latency less than the first latency, the second memory operable to supply data to the processor responsive to processor data requests that form a stream type sequential access pattern; and

the cache-second memory coupled to the prefetch unit, wherein the prefetch unit uses a bit vector to predictively load target cache lines from the system-first memory into the cache memory to reduce an access latency of the processor in preparation for the target cache lines being requested by the processor as part of the stream-type sequential processor access pattern, and wherein the target cache lines are indicated by the stream type sequential access pattern identified by the trackers.

10. (Original) The apparatus of claim 9, wherein each of the trackers include a tag to recognize accesses to cache lines by the processor.

11. (Currently amended) The apparatus of claim 9, wherein a plurality of system first memory accesses by the processor are used by the trackers to determine the target cache lines for a predictive load into the cache-second memory.

12. (Currently amended) The apparatus of claim 11, wherein consecutive accesses by the processor to adjacent cache lines of a page are used to determine the target cache line for a predictive load into the ~~cache-second~~ memory, wherein the adjacent cache lines have adjacent addresses.

13. (Currently amended) The apparatus of claim 9, wherein the ~~system-first~~ memory comprises a plurality of 4KB pages.

14. (Previously presented) The apparatus of claim 9, wherein each of the plurality of trackers is configured to monitor a sub portion of a page for accesses by the processor.

15. (Original) The apparatus of claim 14, wherein the cache lines are 128 byte cache lines and wherein a tag is used to monitor half of a page for accesses by the processor.

16. (Currently amended) The apparatus of claim 9, wherein the ~~cache-second~~ memory is a prefetch cache memory within the prefetch unit.

17. (Currently amended) The apparatus of claim 9, wherein the ~~cache-second~~ memory is an L2 cache memory.

18. (Previously Presented) A method for request tracking data prefetching for a computer system, comprising:

monitoring data transfers between a ~~high latency~~first memory having a first latency and a ~~low latency~~second memory coupled to a processor by using a prefetcher, wherein the first memory has a first latency and the second memory has a second latency less than the first latency, and wherein the prefetcher is coupled to the ~~high latency~~first memory, wherein the ~~low latency~~second memory is a cache memory operable to supply data to the processor responsive to processor data requests;

using a bit vector to track multiple stream-type sequential processor access patterns between the ~~high latency~~first memory and the ~~low latency~~second memory; prefetching data from the ~~high latency~~first memory to the ~~low latency~~second memory as indicated by the stream type sequential processor access patterns in preparation for the data being requested by the processor as part of the stream type processor access pattern and reducing a data access latency of the processor of the computer system.

19. (Currently amended) The method of claim 18 wherein the computer system includes a plurality of processors, and wherein each of the processors is coupled to a respective ~~high latency~~first memory and a ~~low latency~~second memory.

20. (Currently amended) The method of claim 18, wherein consecutive accesses by the processor to adjacent cache lines of the ~~high latency~~first memory are used to determine a target cache line of a stream type access pattern for a prefetching to the ~~low latency~~second memory, wherein the adjacent cache lines have adjacent addresses, and wherein the target cache line is part of stream-type accesses that formed the stream-type access pattern.

21. (Currently amended) The apparatus of Claim 9, wherein said prefetch unit accesses to ~~system~~first memory are timed to utilize processor-to-system memory idle time.

22. (Currently amended) A device for request tracking data prefetching for a computer system, comprising:

means for monitoring data transfers between a ~~high latency~~first memory, ~~having a first latency~~, and a ~~low latency~~second memory coupled to a processor, wherein the ~~low latency~~second memory is a cache memory operable to supply data to the processor responsive to processor data requests, ~~and wherein the second memory has a second latency less than the first latency;~~

means for using a bit vector to track multiple stream-type sequential processor access patterns between the ~~high latency~~first memory and the ~~low latency~~second memory;

means for prefetching data from the ~~high latency~~first memory to the ~~low latency~~second memory as indicated by the stream type sequential processor access patterns in preparation for the data being requested by the processor as part of the stream type processor access pattern and wherein the means for prefetching data is operable to reduce data access latency of the processor of the computer system.

23. (Currently amended) The device of claim 22 wherein the computer system includes a plurality of processors, and wherein each of the processors is coupled to a respective ~~high latency~~first memory and a ~~low latency~~second memory.

24. (Currently amended) The device of claim 22, wherein consecutive accesses by the processor to adjacent cache lines of the ~~high latency~~first memory are used to determine a target cache line of a stream type access pattern for a prefetching to the ~~low latency~~memory~~second~~, wherein the adjacent cache lines have adjacent addresses, and wherein the target cache line is part of stream-type accesses that formed the stream-type access pattern.

25. (New) The apparatus of claim 1, wherein the prefetcher comprises a prefetch cache operable to be used to load of a cache line for the first memory.